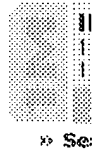


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L11	42	(detect\$3 near5 (fault\$1 or error\$1 or defect\$1)) and ((IC or (integrated adj2 circuit\$1) or chip\$1 or dice\$1) near2 test\$4) and (product near3 vector\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/24 14:35
L12	72	(detect\$3 near5 (fault\$1 or error\$1 or defect\$1)) and ((IC or (integrated adj2 circuit\$1) or chip\$1 or dice\$1) near5 test\$4) and (optimal near2 test\$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/24 14:36
L13	49	(detect\$3 near5 (fault\$1 or error\$1 or defect\$1)) and ((IC or (integrated adj2 circuit\$1) or chip\$1 or dice\$1) near5 test\$4) and (optimal near2 test\$3) and vector\$1	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/24 14:37
L14	6	(detect\$3 near5 (fault\$1 or error\$1 or defect\$1)) and ((IC or (integrated adj2 circuit\$1) or chip\$1 or dice\$1) near5 test\$4) and (select\$3 near5 optimal near5 test\$3) and vector\$1	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/24 14:38
L15	6	(detect\$3 near5 (fault\$1 or error\$1 or defect\$1)) and ((IC or (integrated adj2 circuit\$1) or chip\$1 or dice\$1) near5 test\$4) and (select\$4 near5 optimal near5 test\$3) and vector\$1	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/24 14:38

L16	1	(detect\$3 near5 (fault\$1 or error\$1 or defect\$1)) and ((IC or (integrated adj2 circuit\$1) or chip\$1 or dice\$1) near5 test\$4) and (select\$4 near5 optimal near5 test\$3) and (vector\$1 near3 product\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/24 14:41
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Sayil, S.; Kerns, D.V.; Kerns, S.E.;

Potentials, IEEE , Volume: 24 , Issue: 1 , Feb.-March 2005

Pages:25 - 28

[\[Abstract\]](#)
[\[PDF Full-Text \(634 KB\)\]](#)
IEEE JNL
2 Modeling ESD protection
Mohan, N.; Kumar, A.;

Potentials, IEEE , Volume: 24 , Issue: 1 , Feb.-March 2005

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[\[Abstract\]](#)
[\[PDF Full-Text \(920 KB\)\]](#)
IEEE JNL
3 Mixed mode integrated circuits
Bhadri, P.R.; Srinivasan, R.; Mal, P.; Beyette, F.R., Jr.; Carter, H.W.;

Potentials, IEEE , Volume: 24 , Issue: 1 , Feb.-March 2005

Pages:6 - 11

[\[Abstract\]](#)
[\[PDF Full-Text \(1450 KB\)\]](#)
IEEE JNL
4 Evaluation of SiO/sub 2/ antifuse in a 3D-OTP memory
Feng Li; Xiaoyu Yang; Meeks, A.T.; Shearer, J.T.; Le, K.Y.;

Device and Materials Reliability, IEEE Transactions on , Volume: 4 , Issue: 3 , 2004

Pages:416 - 421

[\[Abstract\]](#)
[\[PDF Full-Text \(1200 KB\)\]](#)
IEEE JNL
5 Diagnosing arbitrary defects in logic designs using single location at

time (SLAT)*Huisman, L.M.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 23 , Issue: 1 , Jan. 2004

Pages:91 - 101

[\[Abstract\]](#) [\[PDF Full-Text \(344 KB\)\]](#) [IEEE JNL](#)**6 On-chip rise-time measurement***Lin, S.L.; Mourad, S.;*

Instrumentation and Measurement, IEEE Transactions on , Volume: 53 , Issue: 6 , Dec. 2004

Pages:1510 - 1516

[\[Abstract\]](#) [\[PDF Full-Text \(1048 KB\)\]](#) [IEEE JNL](#)**7 The boundary scan***Burgess, R., Jr.; Nagaraj, P.; Waseq, M.N.;*

Potentials, IEEE , Volume: 14 , Issue: 3 , Aug.-Sept. 1995

Pages:11 - 12

[\[Abstract\]](#) [\[PDF Full-Text \(268 KB\)\]](#) [IEEE JNL](#)**8 Test set embedding for deterministic BIST using a reconfigurable interconnection network***Lei Li; Chakrabarty, K.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 23 , Issue: 9 , Sept. 2004

Pages:1289 - 1305

[\[Abstract\]](#) [\[PDF Full-Text \(904 KB\)\]](#) [IEEE JNL](#)**9 Test and measurement [Technology 2000 analysis and forecast]***Bretz, E.A.;*

Spectrum, IEEE , Volume: 37 , Issue: 1 , Jan. 2000

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Spectrum, IEEE , Volume: 36 , Issue: 7 , July 1999

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[\[Abstract\]](#) [\[PDF Full-Text \(780 KB\)\]](#) [IEEE JNL](#)**11 Testability on TAP***Maunder, C.M.; Tulloss, R.E.;*

Spectrum, IEEE , Volume: 29 , Issue: 2 , Feb. 1992

Pages:34 - 37

[\[Abstract\]](#) [\[PDF Full-Text \(516 KB\)\]](#) [IEEE JNL](#)

12 Iddq testing for CMOS VLSI*Rajsuman, R.;*

Proceedings of the IEEE , Volume: 88 , Issue: 4 , April 2000

Pages:544 - 568

[\[Abstract\]](#) [\[PDF Full-Text \(1636 KB\)\]](#) [IEEE JNL](#)**13 Applications of asynchronous circuits***Van Berkel, C.H.; Josephs, M.B.; Nowick, S.M.;*

Proceedings of the IEEE , Volume: 87 , Issue: 2 , Feb. 1999

Pages:223 - 233

[\[Abstract\]](#) [\[PDF Full-Text \(252 KB\)\]](#) [IEEE JNL](#)**14 FPGA as Process Monitor-an effective method to characterize poly CD variation and its impact on product performance and yield***Xiao-Yu Li; Feng Wang; La, T.; Zhi-Min Ling;*

Semiconductor Manufacturing, IEEE Transactions on , Volume: 17 , Issue: 3 , 2004

Pages:267 - 272

[\[Abstract\]](#) [\[PDF Full-Text \(1080 KB\)\]](#) [IEEE JNL](#)**15 Defect and error tolerance in the presence of massive numbers of defects***Breuer, M.A.; Gupta, S.K.; Mak, T.M.;*

Design & Test of Computers, IEEE , Volume: 21 , Issue: 3 , May-June 2004

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[\[Abstract\]](#) [\[PDF Full-Text \(216 KB\)\]](#) [IEEE JNL](#)

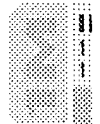
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1 Multiple-parameter CMOS IC testing with increased sensitivity for I/DDQ/
Keshavarzi, A.; Roy, K.; Hawkins, C.F.; De, V.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 11 , Issue: 5 , Oct. 2003

Pages:863 - 870

[\[Abstract\]](#) [\[PDF Full-Text \(480 KB\)\]](#) **IEEE JNL**
2 Defect-oriented testing and defective-part-level prediction
Dworak, J.; Wicker, J.D.; Lee, S.; Grimaila, M.R.; Mercer, M.R.; Butler, K.M.; Stewart, B.; Wang, L.-C.;

Design & Test of Computers, IEEE , Volume: 18 , Issue: 1 , Jan.-Feb. 2001

Pages:31 - 41

[\[Abstract\]](#) [\[PDF Full-Text \(640 KB\)\]](#) **IEEE JNL**
3 RP-SYN: synthesis of random pattern testable circuits with test point insertion
Touba, N.A.; McCluskey, E.J.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 , Issue: 8 , Aug. 1999

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[\[Abstract\]](#) [\[PDF Full-Text \(200 KB\)\]](#) **IEEE JNL**
4 Analog fault diagnosis based on ramping power supply current signal clusters
Somayajula, S.A.S.; Sanchez-Sinencio, E.; Pineda de Gyvez, J.;

Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transacti

[see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Vol 43 , Issue: 10 , Oct. 1996
Pages:703 - 712

[\[Abstract\]](#) [\[PDF Full-Text \(924 KB\)\]](#) [IEEE JNL](#)

5 On the effect of defect clustering on test transparency and IC test optimization

Singh, A.D.; Krishna, C.M.;

Computers, IEEE Transactions on , Volume: 45 , Issue: 6 , June 1996
Pages:753 - 757

[\[Abstract\]](#) [\[PDF Full-Text \(424 KB\)\]](#) [IEEE JNL](#)

6 Modeling of real defect outlines and parameter extraction using a checkerboard test structure to localize defects

Hess, C.; Stroele, A.P.;

Semiconductor Manufacturing, IEEE Transactions on , Volume: 7 , Issue: 3 , A 1994

Pages:284 - 292

[\[Abstract\]](#) [\[PDF Full-Text \(768 KB\)\]](#) [IEEE JNL](#)

7 Minimizing production test time to detect faults in analog circuits

Milor, L.; Sangiovanni-Vincentelli, A.L.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 13 , Issue: 6 , June 1994

Pages:796 - 813

[\[Abstract\]](#) [\[PDF Full-Text \(1608 KB\)\]](#) [IEEE JNL](#)

8 Fault detection in CMOS circuits by consumption measurement

Jacomino, M.; Rainard, J.-L.; David, R.;

Instrumentation and Measurement, IEEE Transactions on , Volume: 38 , Issue 3 , June 1989

Pages:773 - 778

[\[Abstract\]](#) [\[PDF Full-Text \(476 KB\)\]](#) [IEEE JNL](#)

9 Low voltage built-in current sensor

Kuen-Jong Lee; Kou-Shung Huang; Min-Cheng Huang;

Electronics Letters , Volume: 32 , Issue: 21 , 10 Oct. 1996

Pages:1942 - 1943

[\[Abstract\]](#) [\[PDF Full-Text \(224 KB\)\]](#) [IEEE JNL](#)

10 Supply current testing in linear bipolar ICs

Papakostas, D.K.; Hatzopoulos, A.A.;

Electronics Letters , Volume: 30 , Issue: 2 , 20 Jan. 1994

Pages:128 - 130

[\[Abstract\]](#) [\[PDF Full-Text \(280 KB\)\]](#) [IEEE JNL](#)

11 Dynamic I_{dd} test circuit for mixed signal ICs*Arguelles, J.; Martinez, M.; Bracho, S.;*

Electronics Letters , Volume: 30 , Issue: 6 , 17 March 1994

Pages:485 - 486

[\[Abstract\]](#) [\[PDF Full-Text \(152 KB\)\]](#) **IEE JNL****12 Depth profiling by phase shift detection in scanning electron-acous microscopy***Marty-Dessus, D.; Franceschi, J.L.;*

Electronics Letters , Volume: 29 , Issue: 10 , 13 May 1993

Pages:843 - 844

[\[Abstract\]](#) [\[PDF Full-Text \(212 KB\)\]](#) **IEE JNL****13 A DFT technique for delay fault testability and diagnostics in 32-bit performance CMOS ALUs***Chatterjee, B.; Sachdev, M.; Keshavarzi, A.;*

Test Conference, 2004. Proceedings. International , 26-28 Oct. 2004

Pages:1108 - 1117

[\[Abstract\]](#) [\[PDF Full-Text \(947 KB\)\]](#) **IEEE CNF****14 Built-in current sensor for ΔI testing of deep submicron digital CMOS ICs***Vazquez, J.R.; Pineda de Gyvez, J.;*

VLSI Test Symposium, 2004. Proceedings. 22nd IEEE , 25-29 April 2004

Pages:53 - 58

[\[Abstract\]](#) [\[PDF Full-Text \(1401 KB\)\]](#) **IEEE CNF****15 A novel 5GHz RF power detector***Tao Zhang; Eisenstadt, W.R.; Fox, R.M.;*

Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on , Volume: 1 , 23-26 May 2004

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